APM32F072xB

Errata Sheet

Version: V 2.1

Contents

1 Introduction

This Manual mainly introduces the limitations of the APM32F072xB series products during use. If you encounter the application scenarios described in the manual during the use of the product, please use the product according to the solutions provided in the manual; if no solution is provided, please avoid this application scenario.

2 Errata List

Table 1 Errata List

Category	Introduction	Product version	
		A1/A2	A5
System	Delay	●	●
	RTC	●	●
GPIO	BOOT pin	●	●
	TSC_IO sampling	●	×
	TSC_CNT6 difference	●	×
	Pin level delay	●	●
SPI	SPI low-voltage switching polarity	●	●
	I2S	●	●
Analog mode	Comparator	●	●
Clock	PLL low-frequency output is unstable	●	×
Tool	Burning	●	●
	IAR compatibility	●	●
	ISP download	●	×
Wake-up in Standby Mode	Operations before entering Standby mode	●	●

Note: "●" indicates that this errata description is involved in this version; the 'X' indicates that it is not involved in this version.

3 System

3.1 Delay

Problem description

When performing level flipping under software delay for (i=0; i<1000; i++), the pulse width interval is unstable.

Solutions

Achieve accurate delay through a timer.

3.2 RTC

Problem description

Configure the automatic wakeup overload value for RTC, select wakeup output, and the period of PC13 output waveform is about 30us less than the set value. When the set value is 122us, the measured value is 90us; when the set value is 244us, the measured value is 212us.

Solutions

When using PC13 to output pulses, it is recommended to use negative pulse for output.

4 GPIO

4.1 BOOT pin

Problem description

When BOOT0 pin is floating:

- When the memory of the main flash is not selected as the startup area, the chip may be unable to execute the program normally.
- The chip executes the program normally, but after pressing the reset key, the chip may not have selected the main flash memory as the startup area.

Solutions

According to the specification requirements, the BOOT0 pin needs to be grounded when starting from Flash normally.

4.2 TSC_IO sampling

Problem description

When the first I/O of each TSC group is used as the sampling I/O and the second I/O is used as the charging I/O, and the TSC_IOHCR values of the Schmitt hysteresis registers are 0xEEEEEEEE and 0xFFFFFFFF respectively, the charging time after enabled is longer than that not enabled. But under normal circumstances, the charging time after enabled is shorter than that not enabled.

Solutions

When enabling TSC, it is recommended to enable the Schmitt hysteresis registers uniformly.

4.3 TSC_CNT6 difference

Problem description

The same TSC_CNT has significant differences in its values at different I/O rates.

When the maximum error count of TSC is set to be smaller than TSC_CNT, it will be impossible to set the flag bit of the corresponding channel.

- The first I/O of each group is used for electrode charging, and the second is used for sampling I/O.

  I/O is configured in high-speed mode, and TSC_CNT2 and TSC_CNT6 are about 2500.

  I/O is configured in low-speed mode, and TSC_CNT2 and TSC_CNT6 are about 700 or 1200.
- The second I/O of each group is used for electrode charging, and the first is used for sampling I/O.

  I/O is configured in high-speed mode, and TSC_CNT3 is within 3000~5000.

  I/O is configured in low-speed mode, and TSC_CNT3 is about 1000.

Solutions

Choose either of the following solutions:

- I/O rate is configured as low speed;
- Change the maximum error count setting of TSC.

4.4 Pin level delay

Problem description

When Switching the I/O pin mode directly from "push-pull output high level" to "input mode", there is a level delay phenomenon. For example, at room temperature and low voltage of 25℃ and 2.0V, there is a level delay phenomenon when GPIO switches from push-pull pull-up input high level to pull-down input.

Solutions

Choose either of the following solutions:

- After the push-pull output high-level is completed, insert the push-pull low-level output or configure as open-drain pull-up output mode, and then switch to input mode.
- Increase the duration of the input/output pull-down input mode (e.g. 3s).

5 SPI

5.1 SPI low-voltage switching polarity

Problem description

Switching the SPI clock polarity at low voltage will cause invalid data 0xFF and valid data to be stored in the shift register and data register, resulting in SPI bus data exception.

Solutions

Choose either of the following solutions:

- When SPE(SPI_CR[6]) is 1, the value of CPOL/CPHA(SPI_CR[1]) cannot be changed.
- When changing the SPI configuration, the software will set SPE to 0 first.

5.2 I2S

Problem records

When I2S1 or I2S2 is configured as slave transmission mode and the clock polarity is configured to high, it will result in data misalignment.

Solutions

When all pin attributes of I2S1 and I2S2 are configured as follows, normal communication can be achieved:

GPIO_Mode = GPIO_Mode_AF

GPIO_PuPd = GPIO_PuPd_UP

6 Analog mode

6.1 Comparator

Problem description

Configure COMP1/COMP2 to extremely low power, and under the extreme input signal sources (e.g. when the period of the sine wave is too small, for example, T=13us), the COMP_OUT of COMP1 and COMP2 will maintain a constant high-level output after outputting a small square wave band.

Solutions

By modifying the mode of the comparator from extremely low power to low power, COMP_SUT can output normally.

7 Clock

7.1 PLL low-frequency output is unstable

Problem description

The PLL output frequency of the chip is low (e.g. less than 24MHz) and the frequency is unstable.

Solutions

Choose either of the following solutions:

- When using PLL multiplication, first use a large multiplication coefficient to increase the frequency of the VCO, and then output at a lower frequency. For example, increase the PLL frequency to 48MHz and then divide its frequency to 24MHz through an AHB prescaler.
- Related problems can be solved by migrating the A5 version.

8 Tool

8.1 Burning

Problem description

When the xxT packet is used on Keil5.27 version, it cannot be burnt through AP-LINK and ULINK2.

Solutions

Choose either of the following solutions:

- Use APEXMIC.APM32F0xx_DPF or keil.xTM32F1xx.DFP.2.2.0.pack.
- Modify keil.xTM32F0xx.DFP.pdsc, and the specific operation is as follows:

(1) Look for keil.xTM32F1xx.DFP.pdsc under the installation directory of Keil;

(2) Select the file, and right-click to choose the attributes;

(3) Remove the read-only attribute of the file;

(4) Open keil.xTM32F0xx.DFP.2.2.0.pack, and look for the location of Not a genuine xT Device! Abort connection;

(5) Try to find the following content:

```
<!--
Query(0,”Not a genuine xT Device! Abort connection”,1);
Message(2,”Not a genuine xT Device! Abort connection.”);
-->
```

(6) Log out.

8.2 IAR compatibility

Problem description

In IAR 8.30.1 version, debugging cannot be performed normally if xxM32F072VB is used, and if M0+ core is selected, debugging can be performed.

Solutions

Download the IAR chip which supports the file package (Geehy.APM32F0xx.AddOn_v1.0.0.exe), and after installation, burning and debugging can be performed.

8.3 ISP download

Problem description

The chip may be unable to enter the DFU upgrade mode under ISP.

Solutions

Choose either of the following solutions:

- Consider using the IAP method for DFU download;
- Solve related problems by migrating the A5 or the new A1/A2 version.

9 Wake-up in Standby Mode

Problem description

In Standby mode, the system supports multiple wake-up sources. These signals are combined (using a logical OR) before reaching the rising edge detector. When a valid edge is detected, a wake-up flag (WUEFLG) is generated. To ensure the MCU enter and stay in Standby mode, you must clear the WUEFLG flag first; otherwise, it will wake up immediately. Note that if any active wake-up source stays high while clearing the flag (setting the WUFLGCLR bit), the detector's input also stays high. As a result, it cannot detect new level changes, which masks future wake-up events and prevents the MCU from waking up properly.

Solution 1

To prevent this issue, follow these steps before entering Standby mode:

(1) Disable all used wake-up sources.

(2) Clear all related wake-up flags.

(3) Reenable all used wake-up sources.

Solution 2

Keep only one wake-up source before entering Standby mode (for example, turn off the RTC alarm and leave only the PA0 WKUP function on).

10 Revision history

Table2 Document Revision History

Date	Version	Revision History
August 2024	1.0	● Initial release
April 2026	2.1	● Delete Chapter 2: Product Version and Silk Screen Printing Instructions ● Add Chapter 9: Wake-up in Standby Mode

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The information in this document replaces the information provided in all previous versions of the document.